CLAIMS

What is Claimed is:

1. An integrated circuit package comprising:

a package substrate having a top and a bottom;

a plurality of bypass capacitors coupled to said bottom without a cavity; and

an array of solder balls formed on said bottom, wherein said array of solder balls facilitates surface mounting to a printed circuit board assembly, and wherein said solder balls provide sufficient space between said printed circuit board assembly and said bypass capacitors.

2. The integrated circuit package as recited in Claim 1 wherein said package substrate comprises an organic substrate.

3. The integrated circuit package as recited in Claim 1 further comprising a chip die coupled to said top in a flip-chip configuration.

4. The integrated circuit package as recited in Claim 1 further comprising a chip die coupled to said top in a wire bonding configuration.

5. The integrated circuit package as recited in Claim 1 wherein a height of each solder ball is approximately 0.5 millimeters.

6. The integrated circuit package as recited in Claim 1 wherein a height of each bypass capacitor is approximately between 0.325 millimeters and 0.350 millimeters.

7. The integrated circuit package as recited in Claim 1 wherein a portion of said bypass capacitors are coupled within a center of said bottom.

8. An electronic assembly comprising:

a printed circuit board assembly; and

an integrated circuit package surface mounted to said printed circuit board assembly, wherein said integrated circuit package comprises:

a package substrate having a top and a bottom,

a plurality of bypass capacitors coupled to said bottom without a cavity, and

an array of solder balls formed on said bottom, wherein said array of solder balls facilitates a surface mounting technique, and wherein said solder balls provide sufficient space between said printed circuit board assembly and said bypass capacitors.

9. The electronic assembly as recited in Claim 8 wherein said package substrate comprises an organic substrate.

10. The electronic assembly as recited in Claim 8 wherein said integrated circuit package further comprises a chip die coupled to said top in a flip-chip configuration.

11. The electronic assembly as recited in Claim 8 wherein said integrated circuit package further comprises a chip die coupled to said top in a wire bonding configuration.

12. The electronic assembly as recited in Claim 8 wherein a height of each solder ball is approximately 0.5 millimeters.

13. The electronic assembly as recited in Claim 8 wherein a height of each bypass capacitor is approximately between 0.325 millimeters and 0.350 millimeters.

14. A method of surface mounting an integrated circuit package having a package substrate to a printed circuit board assembly, said method comprising:

forming an array of solder balls on a bottom of said package substrate;

coupling a plurality of bypass capacitors to said bottom without a cavity; and

using said array of solder balls to surface mount said integrated circuit package to said printed circuit board assembly, and wherein said solder balls provide sufficient space between said printed circuit board assembly and said bypass capacitors.

15. The method as recited in Claim 14 wherein said package substrate comprises an organic substrate.

16. The method as recited in Claim 14 wherein said integrated circuit package further comprises a chip die coupled to a top of said package substrate in a flip-chip configuration.

17. The method as recited in Claim 14 wherein said integrated circuit package further comprises a chip die coupled to a top of said package substrate in a wire bonding configuration.

18. The method as recited in Claim 14 wherein a height of each solder ball is approximately 0.5 millimeters.

19. The method as recited in Claim 14 wherein a height of each bypass capacitor is approximately between 0.325 millimeters and 0.350 millimeters.

20. The method as recited in Claim 14 wherein said coupling said plurality of bypass capacitors includes:

coupling a portion of said bypass capacitors within a center of said bottom.

21. The method as recited in Claim 14 further comprising:

performing a reflow process after forming said array of solder balls and coupling said bypass capacitors.